said resistance element comprising:

a first resistance pattern provided on said substrate at a first level; and

a second resistance pattern provided adjacent to said first resistance pattern at a second level lower than said first level, said second resistance pattern being connected in series to said first resistance pattern,

said second resistance pattern having an edge defined by said first resistance pattern.

7. (Amended) A semiconductor device as claimed in claim 1, wherein said second resistance pattern is formed on a device isolation film covering said substrate, said second resistance pattern including a first polysilicon pattern provided on said insulation film and a polycide region formed on a surface part of said first polysilicon pattern defined by said first resistance pattern.

REMARKS

The application has been reviewed in light of the Office Action dated August 1, 2001. Claims 1-9 are pending in this application, with claim 1 being in independent form and claim 8 withdrawn from consideration. By the present Amendment, claims 1 and 7 have been amended. It is submitted that no new matter has been added and no new issues have been raised by the present Amendment.

A Request For Approval to Make Drawing Changes is submitted herewith to label Fig. 1 as "Prior Art" as requested in the Office Action. In addition, the Examiner's attention is directed to Fig. 2E for element 10A as described in the specification. Withdrawal of the

objection to the drawings is respectfully requested.

Claims 1-8 were rejected under 35 U.S.C. §112, second paragraph, as allegedly indefinite. In response, claim 1 has been amended to address the formal points raised in the Office Action only. It is noted that claims 7 and 8 are directed to the embodiments shown in Figs. 5A, 5B. Of course, the claims are not limited to the disclosed embodiments. Withdrawal of the rejection under Section 112, second paragraph, is respectfully requested.

Claims 1-3 and 5-8 were rejected under 35 U.S.C. §102(b) as allegedly anticipated by U.S. Patent 5,621,232 to Ohno. Claims 1-3, 5, 7 and 8 were also rejected under Section 102(b) as allegedly anticipated by U.S. Patent 4,804,636 to Groover III, et al. Claims 1-5, 7 and 8 were also rejected under 35 U.S.C. §103(a) as allegedly obvious from U.S. Patent 5,911,114 to Naem. Applicants have carefully considered the Examiner's comments and the cited art, and respectfully submit independent claim 1 is patentably distinct from the cited art, for at least the following reasons.

The present disclosure is directed to semiconductor devices having an integral resistance element. A second resistance pattern is provided adjacent to a first resistance pattern at a second level lower than the first level of the first resistance pattern, the second resistance pattern being connected in series to the first resistance pattern and the second resistance pattern having an edge defined by the first resistance pattern. The claimed structure allows for the variation of the total resistance of the resistance elements to be effectively compensated for (page 13, lines 11-22).

Ohno, as understood by Applicants, relates to a semiconductor device including a local interconnection between an interconnection layer and an adjoining impurity region.

However, Ohno is not understood to be concerned with integral resistance elements, still less a semiconductor device, comprising a Si substrate and a resistance element formed on the Si substrate, the resistance element comprising a first resistance pattern provided on the substrate at a first level and a second resistance pattern provided adjacent to the first resistance pattern at a second level lower than the first level, the second resistance pattern being connected in series to the first resistance pattern, the second resistance pattern having an edge defined by the first resistance pattern, as recited in claim 1.

Groover, III et al., as understood by Applicants, relates to a process for making integrated circuits having titanium nitride triple interconnect. Groover, III et al. refers to poly layers used for poly-to-poly capacities and/or sometimes resistors (column 19, lines 1-3).

However, Applicant also finds no teaching or suggestion in Groover, III et al. an substrate and a resistance element formed on the Si substrate, the resistance element comprising a first resistance pattern provided on the substrate at a first level and a second resistance pattern provided adjacent to the first resistance pattern at a second level lower than the first level, the second resistance pattern being connected in series to the first resistance pattern, the second resistance pattern having an edge defined by the first resistance pattern.

Accordingly, Applicants submit independent claim 1 is patentably distinct from Ohno and Groover III et al.

Naem, as understood by Applicants relate to a method of simultaneous formation of salicide and local interconnects in an integrated circuit structure.

However, Applicants also find no teaching or suggestion in Naem of an Si substrate and a resistance element formed on the Si substrate, the resistance element comprising a first

resistance pattern provided on the substrate at a first level and a second resistance pattern provided adjacent to the first resistance pattern at a second level lower than the first level, the second resistance pattern being connected in series to the first resistance pattern, the second resistance pattern having an edge defined by the first resistance pattern.

Accordingly, Applicants submit independent claim 1 is also patentable over Naem.

Further, utilizing the presently claimed structure, the pattern size of the lower resistance pattern can be defined by the upper resistance pattern. Accordingly, the width of the first resistance pattern is increased when the width of the second resistance pattern is decreased, or vice versa. Thereby, the variation of overall resistance of the resistance element can be eliminated by connecting the first and second resistance patterns in series.

In contrast, Ohno and Grover III et al. teach the local interconnection connecting the gate and source or gate and drain of a MOS transistor. Thus, there is no teaching at all in the cited art to use the upper and lower patterns such as the patterns 7b and 7a of Ohno, Fig. 2 or the polysilicon patterns of Grover, Fig. 9c, as a resistance pattern.

Further, it is noted that, in Ohno and Grover III et al., the upper pattern and the lower pattern are separated by a sidewall insulation film covering the sidewall of the gate electrode. See any diagram of Ohno or Grover. Accordingly, there is no teaching or suggestion in the cited art of "said second resistance pattern having an edge defined by said first resistance pattern," as recited in independent claim 1.

Without the foregoing features, the advantageous effects of the present disclosure of compensating for the variation of resistance of one resistance pattern by the other resistance pattern can not be achieved.

The Office is hereby authorized to charge any additional fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a petition for an additional extension of time is required to make this response timely, this paper should be considered to be such a petition, and the Commissioner is authorized to charge the requisite fees to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Entry of this amendment and allowance of this application are respectfully requested.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES IN THE CLAIMS

1. (Amended) A semiconductor device, comprising:

a Si substrate; and

a resistance element formed on said Si substrate,

said resistance [pattern] element comprising:

a first resistance pattern provided on said substrate at a first level; and

a second resistance pattern provided adjacent to said [second] first resistance pattern at a second level lower than said first level, said second resistance pattern being connected in series to said first resistance pattern,

said second resistance pattern having an edge defined by said first resistance pattern.

7. (Amended) A semiconductor device as claimed in claim 1, wherein said second resistance pattern is formed on a device isolation film covering said substrate, said second resistance pattern including a first polysilicon pattern provided on said insulation film and a polycide [salicide] region formed on a surface part of said first polysilicon pattern defined by said first resistance pattern.